WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a plurality of wirings formed to extend in a first direction;

memory cells containing nonvolatile memory cell transistors and connected to the plurality of wirings;

word lines commonly connected to gate electrodes of the nonvolatile memory cell transistors arranged along a second direction which intersects the first direction; and

driving circuits respectively connected to the plurality of wirings, each of the driving circuits including a detection circuit which detects threshold voltage of the nonvolatile memory cell transistor in a verify operation, a storage circuit which stores threshold voltage detected by the detection circuit and a potential setting circuit which sets potential of the wiring to at least three potentials based on the threshold voltage stored in the storage circuit in a program operation following the verify operation.

2. The device according to claim 1, wherein the at least three potentials include program inhibition potential used to inhibit a data programming operation, program potential used to perform a data programming operation and program suppression potential which has potential between the program inhibition potential and

the program potential and is used to program data while suppressing a program amount.

3. The device according to claim 2, wherein the threshold voltage of the nonvolatile memory cell transistor is detected by converting at least one of potential applied to the gate electrode of the nonvolatile memory cell transistor, initial charging potential applied to the wiring, determination reference potential to determine the potential of the wiring, and determination reference time to determine the potential of the wiring and performing the verify readout operation at least twice.

4. The device according to claim 3, wherein the storage circuit stores the results of the verify readout operation performed at least twice.

5. The device according to claim 2, wherein the threshold voltage of the nonvolatile memory cell transistor is detected based on time required for the potential of the wiring to reach preset potential in the verify operation.

6. The device according to claim 5, wherein the storage circuit stores time required for the potential of the wiring to have reached the preset potential.

7. The device according to claim 2, wherein the threshold voltage of the nonvolatile memory cell transistor is detected based on the potential of the wiring when preset time has elapsed in the verify

operation.

8. The device according to claim 7, wherein the storage circuit stores the potential of the wiring set when the preset time has elapsed.

9. The device according to claim 2, wherein the at least three potentials are discrete values which are independently set.

10. The device according to claim 3, wherein the at least three potentials are discrete values which are independently set.

11. The device according to claim 5, wherein the at least three potentials are discrete values which are independently set.

12. The device according to claim 7, wherein the at least three potentials are discrete values which are independently set.

13. The device according to claim 2, wherein the program suppression potential is selected from successive values which lie between the program inhibition potential and the program potential based on the threshold voltage information and set to the selected value.

14. The device according to claim 5, wherein the program suppression potential is selected from successive values which lie between the program inhibition potential and the program potential based on the threshold voltage information and set to the

selected value.

15. The device according to claim 7, wherein the program suppression potential is selected from successive values which lie between the program inhibition potential and the program potential based on the threshold voltage information and set to the selected value.

16. The device according to claim 1, wherein the memory cell is a NAND cell.

17. The device according to claim 1, wherein the memory cell is an AND cell.

18. A data programming method of a nonvolatile semiconductor memory device comprising:

programming data into a nonvolatile memory cell transistor,

verifying threshold voltage of the nonvolatile memory cell transistor into which data has been programmed,

setting potential of a bit line to program inhibition potential used to inhibit data programming if it is detected based on the result of verification that a sufficient amount of data has been programmed, and

setting the potential of the bit line to one of program potential used to program data according to the threshold voltage of the nonvolatile memory cell transistor and at least one program suppression

potential which lies between the program inhibition potential and the program potential and is used to program data while suppressing a program amount and additionally programming data into the nonvolatile memory cell transistor if it is detected based on the result of verification that a sufficient amount of data has not been programmed.

19. The method according to claim 18, wherein word line potential is stepped up with respect to word line potential used at the data programming time before the verify operation when data is additionally programmed.

20. The method according to claim 19, wherein a stepped-up range of the word line potential is an integer multiple of a potential difference between the program potential and the program suppression potential.

21. The method according to claim 18, wherein the threshold voltage of the nonvolatile memory cell transistor is determined by setting the word line potential to potential different from verify potential and reading out data.

22. The method according to claim 21, wherein a potential difference between the verify potential and the potential different from the verify potential is equal to a potential difference between the program potential and the program suppression potential.

23. The method according to claim 18, wherein the

threshold voltage of the nonvolatile memory cell transistor is determined based on a period of time in which potential of the bit line reaches preset potential from an initial charging potential after setting the potential of the bit line to the initial charging potential and reading out data.

24. The method according to claim 19, wherein the threshold voltage of the nonvolatile memory cell transistor is determined based on a period of time in which potential of the bit line reaches preset potential from an initial charging potential after setting the potential of the bit line to the initial charging potential and reading out data.

25. The method according to claim 20, wherein the threshold voltage of the nonvolatile memory cell transistor is determined based on a period of time in which potential of the bit line reaches preset potential from an initial charging potential after setting the potential of the bit line to the initial charging potential and reading out data.

26. The method according to claim 21, wherein the threshold voltage of the nonvolatile memory cell transistor is determined based on a period of time in which potential of the bit line reaches preset potential from an initial charging potential after setting the potential of the bit line to the initial charging potential and reading out data.

27. The method according to claim 22, wherein the threshold voltage of the nonvolatile memory cell transistor is determined based on a period of time in which potential of the bit line reaches preset potential from an initial charging potential after setting the potential of the bit line to the initial charging potential and reading out data.

28. The method according to claim 18, wherein the threshold voltage of the nonvolatile memory cell transistor is detected based on potential of the bit line when preset time has elapsed after setting the potential of the bit line to the initial charging potential and reading out data.

29. The method according to claim 19, wherein the threshold voltage of the nonvolatile memory cell transistor is detected based on potential of the bit line when preset time has elapsed after setting the potential of the bit line to the initial charging potential and reading out data.

30. The method according to claim 20, wherein the threshold voltage of the nonvolatile memory cell transistor is detected based on potential of the bit line when preset time has elapsed after setting the potential of the bit line to the initial charging potential and reading out data.

31. The method according to claim 21, wherein the threshold voltage of the nonvolatile memory cell

transistor is detected based on potential of the bit line when preset time has elapsed after setting the potential of the bit line to the initial charging potential and reading out data.

32. The method according to claim 22, wherein the threshold voltage of the nonvolatile memory cell transistor is detected based on potential of the bit line when preset time has elapsed after setting the potential of the bit line to the initial charging potential and reading out data.